16 Channel Programmable Delay

D16G

General Description

The D16G is a custom designed 16-channel programmable delay circuit. Each channel consists of an input LVDS-to-CMOS level converter; four stages of delay with 1, 2, 4, and 8 steps; and output width pulse shaper. Also, the chip has the possibility to generate a test level at each output. This option is used for testing chip-to-chip connections. The chip has a serial interface to control the delay and set the output test level.

The D16G is designed and fabricated using a CMOS 0.5 micron technology.

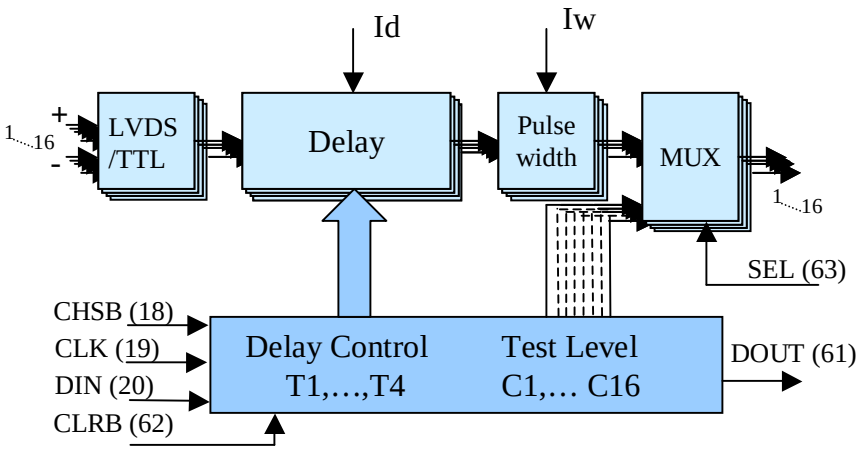
The chip is capsulated into a QFP-64L 10X10 plastic package.

This ASIC is designed as a part of the anode front-end electronics for Cathode Strip Chambers of the Endcap of the Muon System of CMS experiment.

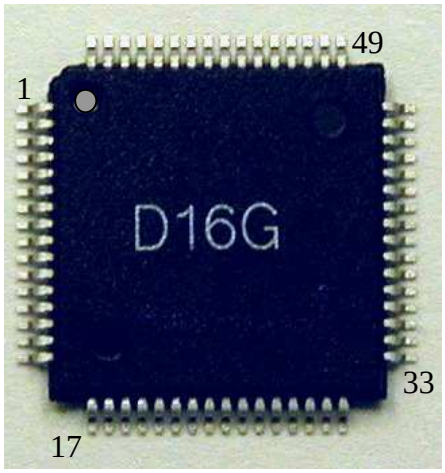
Features

Input signal level	LVDS standard
Input resistance	110 Ohm
Output signal	3.3 V CMOS
Number of delay steps	15
Delay step (slope)	1- 4 ns (adjustable with an external current)
Output pulse width	40 ns (adjustable with an external current)
Power supply voltage	3.3 V
Power consumption	0.2 W
Temperature drift	0.6 ns/10°C

Block Diagram



Top View



Size: 10 mm x 10 mm x 1 mm.

Pin pitch: 0.5 mm.

http://www-hep.phys.cmu.edu/cms/
http://dbserv.pnpi.spb.ru/ofve/red/

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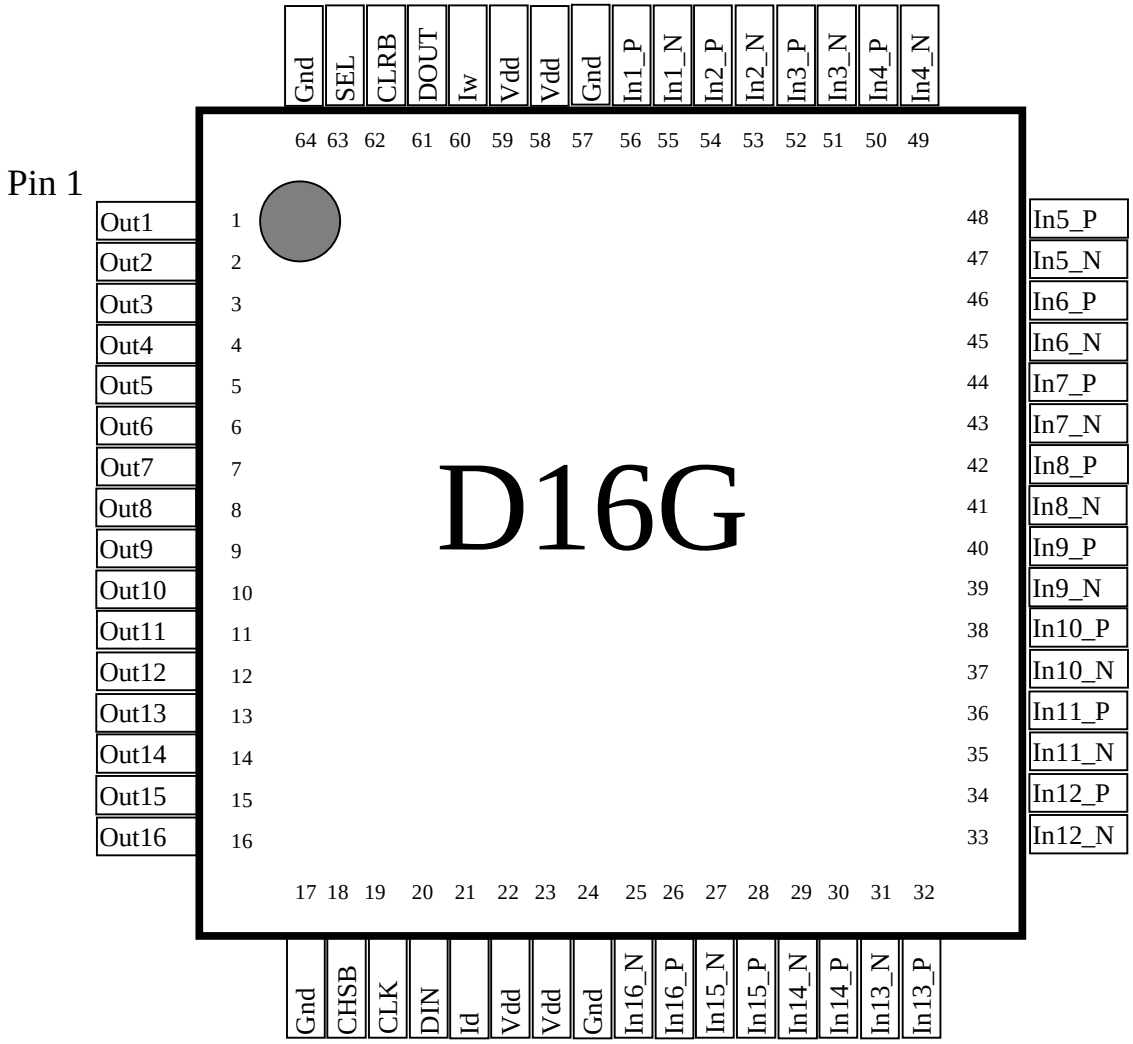
Pin Configuration



Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input signal level				LVDS standard		
Input impedance	**Rinp**			110		Ohm
Output signal				3.3 V CMOS		
Minimum delay	**Tdel.min**	Pin **Id** connected to Gnd via 10K, delay code 0	19	22	24	ns
Delay step (slope)	**Sd**	Adjustable with an external current	1		4	ns/LSB
Number of delay steps				15		
Delay nonlinearity				**Sd**/2		ns
Channel-to-channel difference within chip	**dT**				**Sd**	ns
Output pulse width	**Tpulse**	Pin **Iw** connected to Gnd via 20K.		40		ns
Output pulse rise time		Load capacitance 15 pF		4		ns
Output pulse fall time		Load capacitance 15 pF		4		ns
Output current	**Iout**			15		mA
Power supply voltage	**Vdd**			3.3		V
Power consumption	**P**				0.2	W

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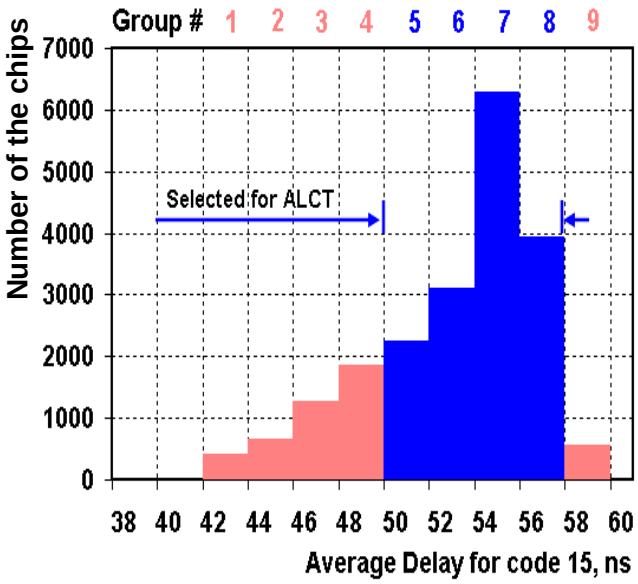
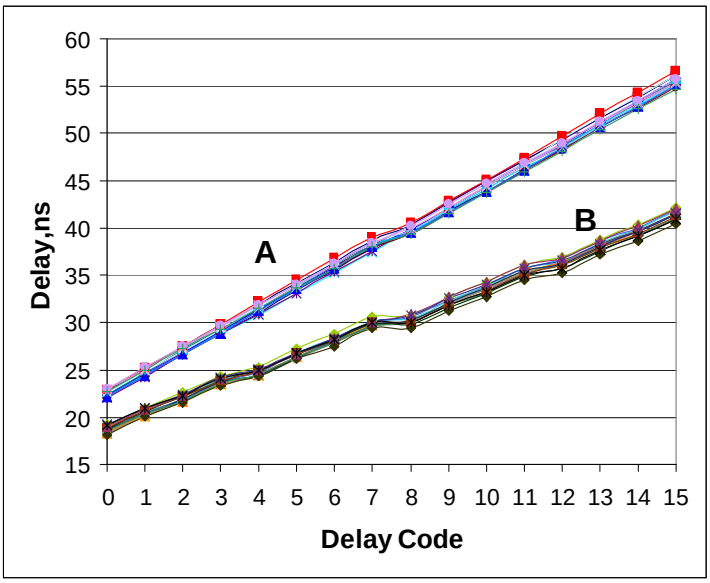
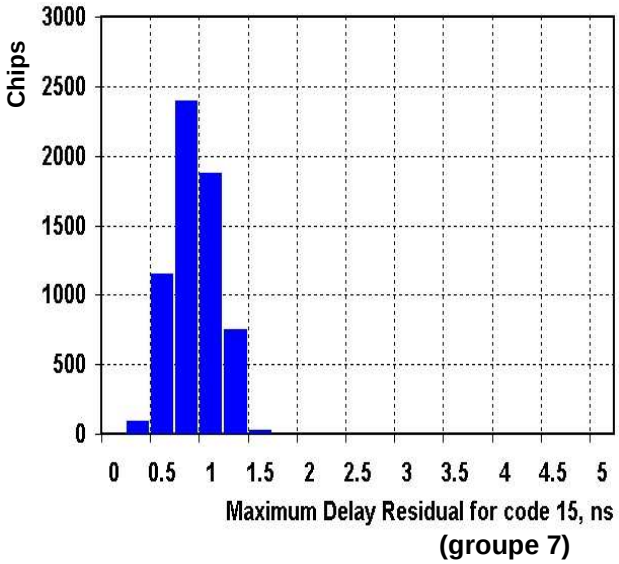
Test Performance

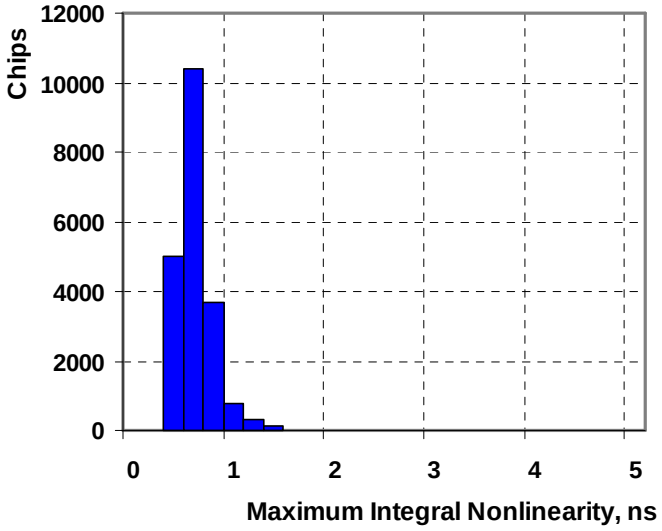


Delay chip distribution vs. delay at code 15.



Typical samples of delay vs. delay code.
A – group 7, delay slope 2.2 ns/LSB
B – group 1, delay slope 1.5 ns/LSB





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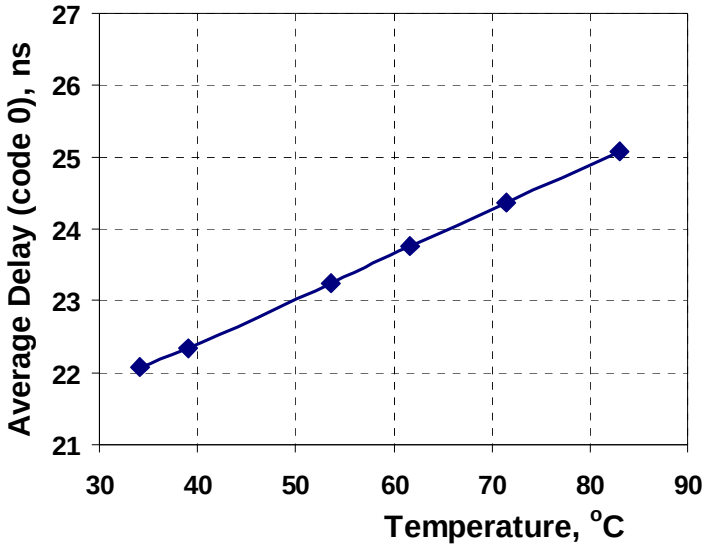
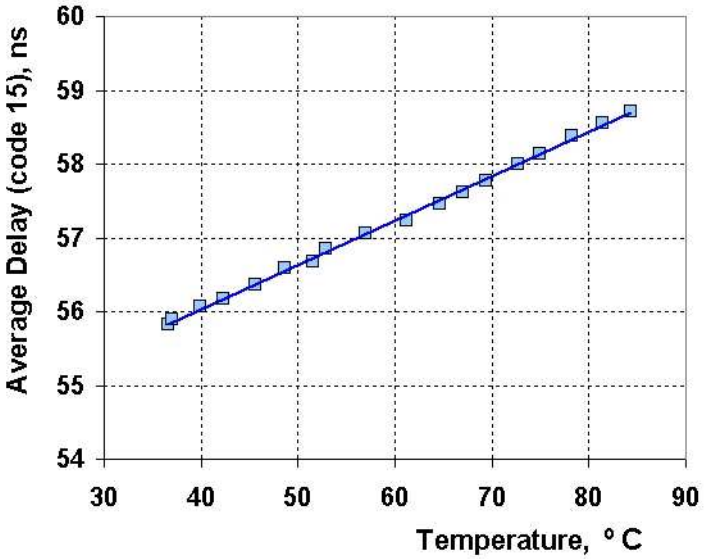
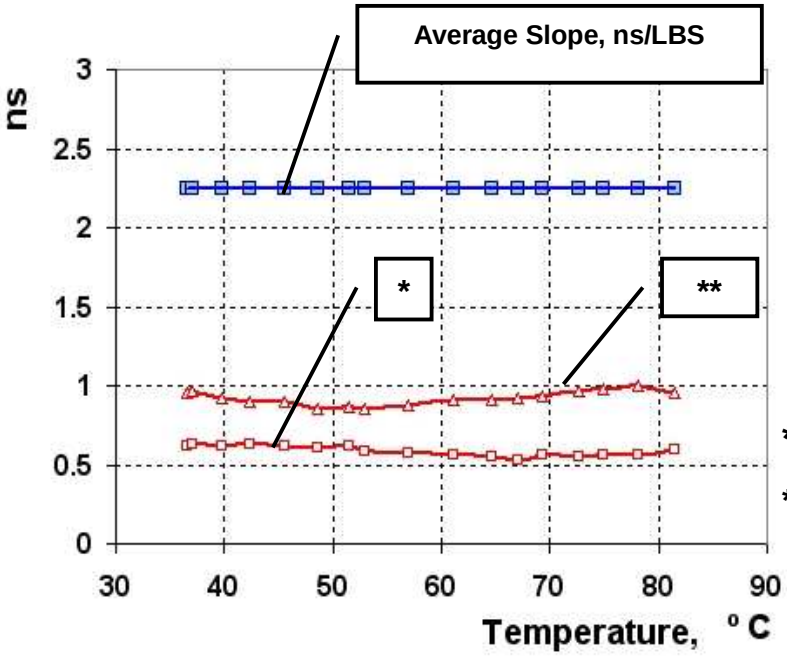
Temperature dependence



Delay vs. temperature (code 0).



Delay vs. temperature (code 15).



Delay slope and residual vs. temperature.

Temperature range 36 ° C - 85 ° C
Delay drift rate - 0.6 ns / 10 ° C

***) Maximum delay residual for code 0**

****) Maximum delay residual for code 15**

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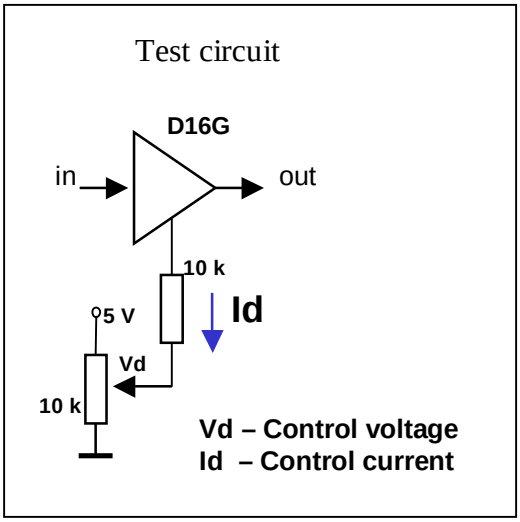
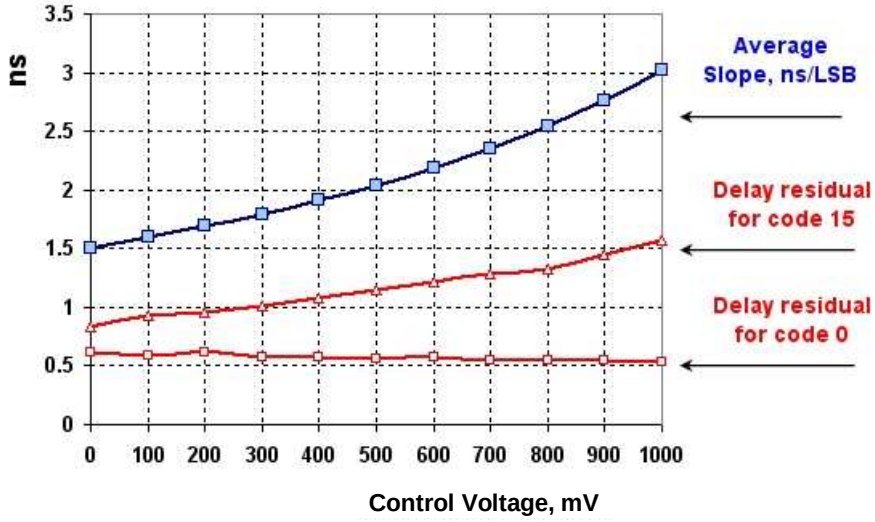
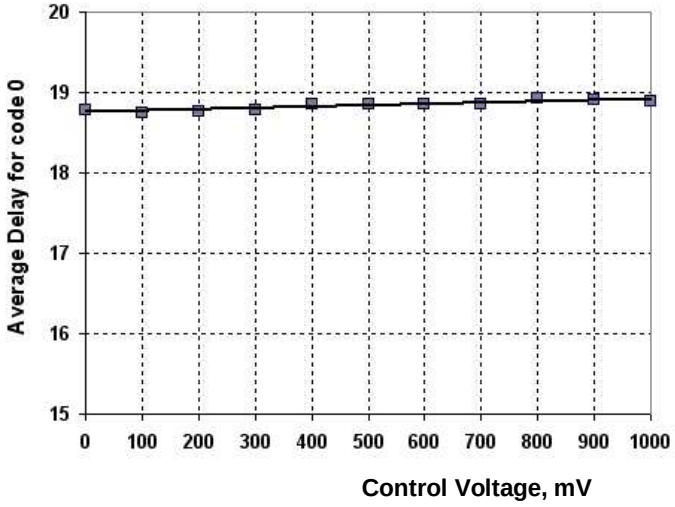
Delay Slope Tuning by Voltage



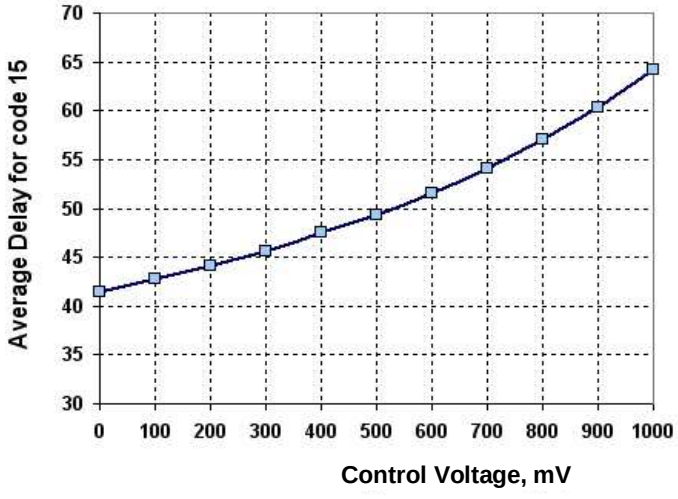


Delay (Va) @ code 0 = constant
Delay (Va) @ code 15 = 1.42 ns / 100 mV
Slope (Va) = 0.10 ns / 100 mV

Delay slope vs. Control Voltage.



Minimum delay (delay code 0) vs. Control Voltage.



Maximum delay (delay code 15) vs. Control Voltage.

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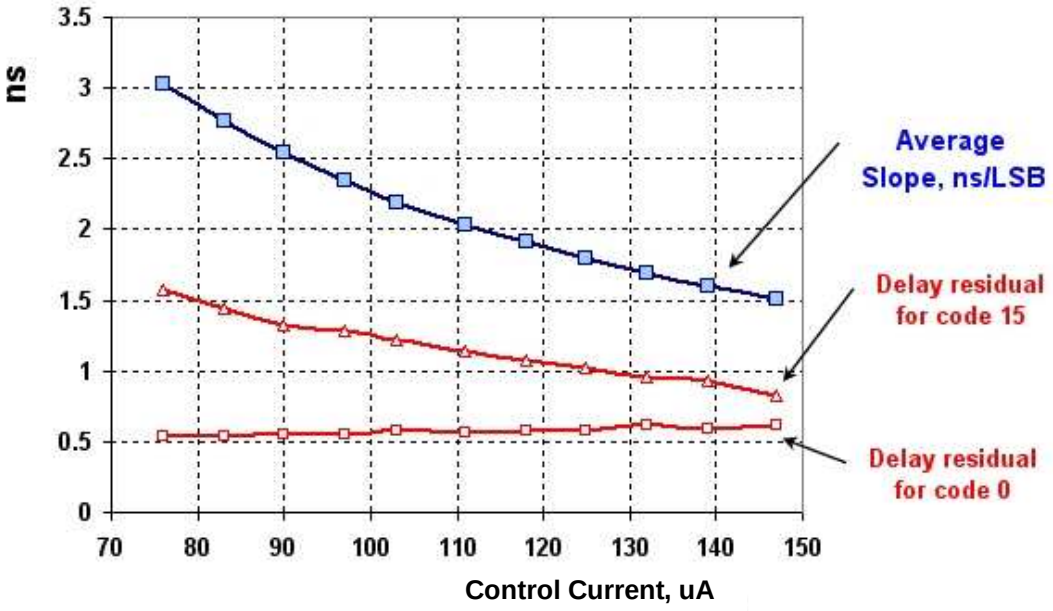
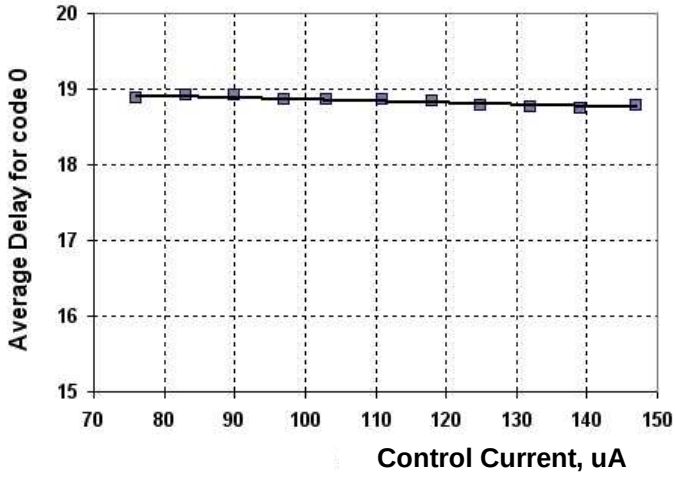
Delay Slope Tuning by Current

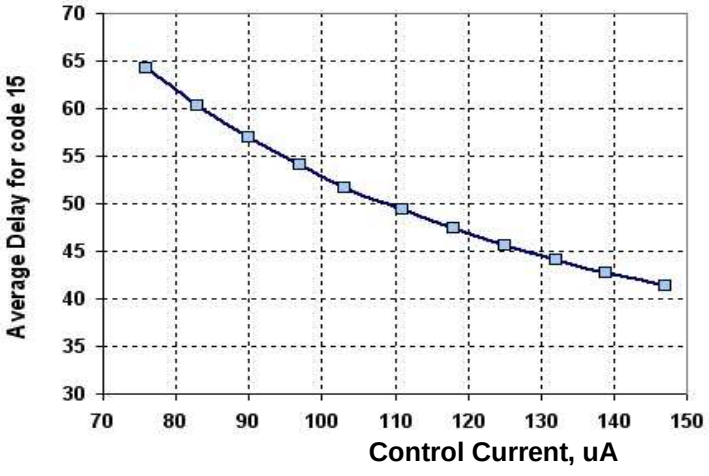


Delay slope vs. Control Current.

Delay (Ia) @ code 0 = constant
Delay (Ia) @ code 15 = - 1.93 ns/ 10 µA
Slope (Ia) = - 0.13 ns / 10 µA



Minimum delay (delay code 0) vs. Control Current.



Maximum delay (delay code 15) vs. Control Current.

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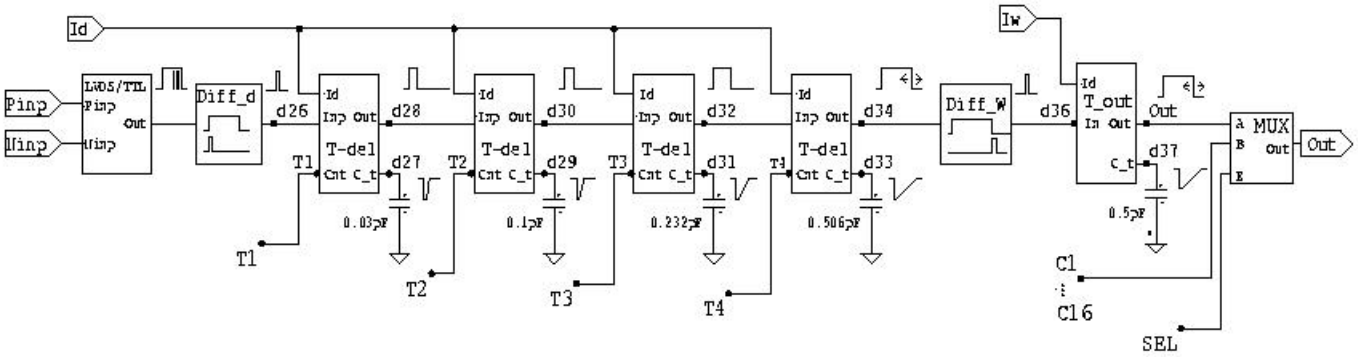
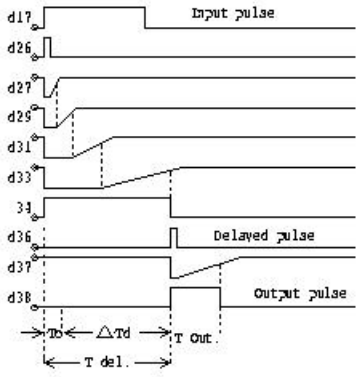
Single-Channel Structure



Time diagram:



Delay for chip:

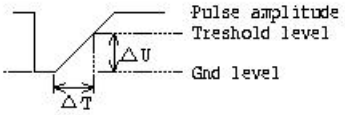
Tdel= To+ △Td

To - minimal delay of the delay circuit

△Td = △ T1+△T2+ △T3+ △T4

Delay for each stage :

△ Ti = Ci* △U/Id, i=1,2,3,4



Output pulse width:

△ Tout = Cout * △ U/Iw

△ U - Trigger Smith threshold

△ Ti - delay time for each stage

Ci - delay capacitors

Cout - Output pulse shaping capacitor

Id - delay circuit charging current

Iw - output pulse shaping capacitor

Multiplexer logic table.

E	A	B	Out
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

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Control Logic

C1, C2, …, C16 test level bits

T1, T2, T3, T4 – delay control