DATA ACQUISITION SYSTEM FOR THE EXPERIMENT “PROTON”

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The “Proton” experiment uses the innovative *ep* elastic scattering method, which allows recording both recoil protons and scattered electrons with high accuracy and resolution, which leads to a completely new approach to measuring the proton radius.

The “Proton” set-up [1] includes two gaseous ionization detectors: an active hydrogen target in the form of an axial time-projection chamber (TPC) detecting recoil protons and a high precision forward tracker (FT) in the form of a set of multiwire proportional chambers with a cathode strip readout that registers scattered electrons. The FT is located behind the TPC in a separate volume of the same vessel, see Fig. 1.

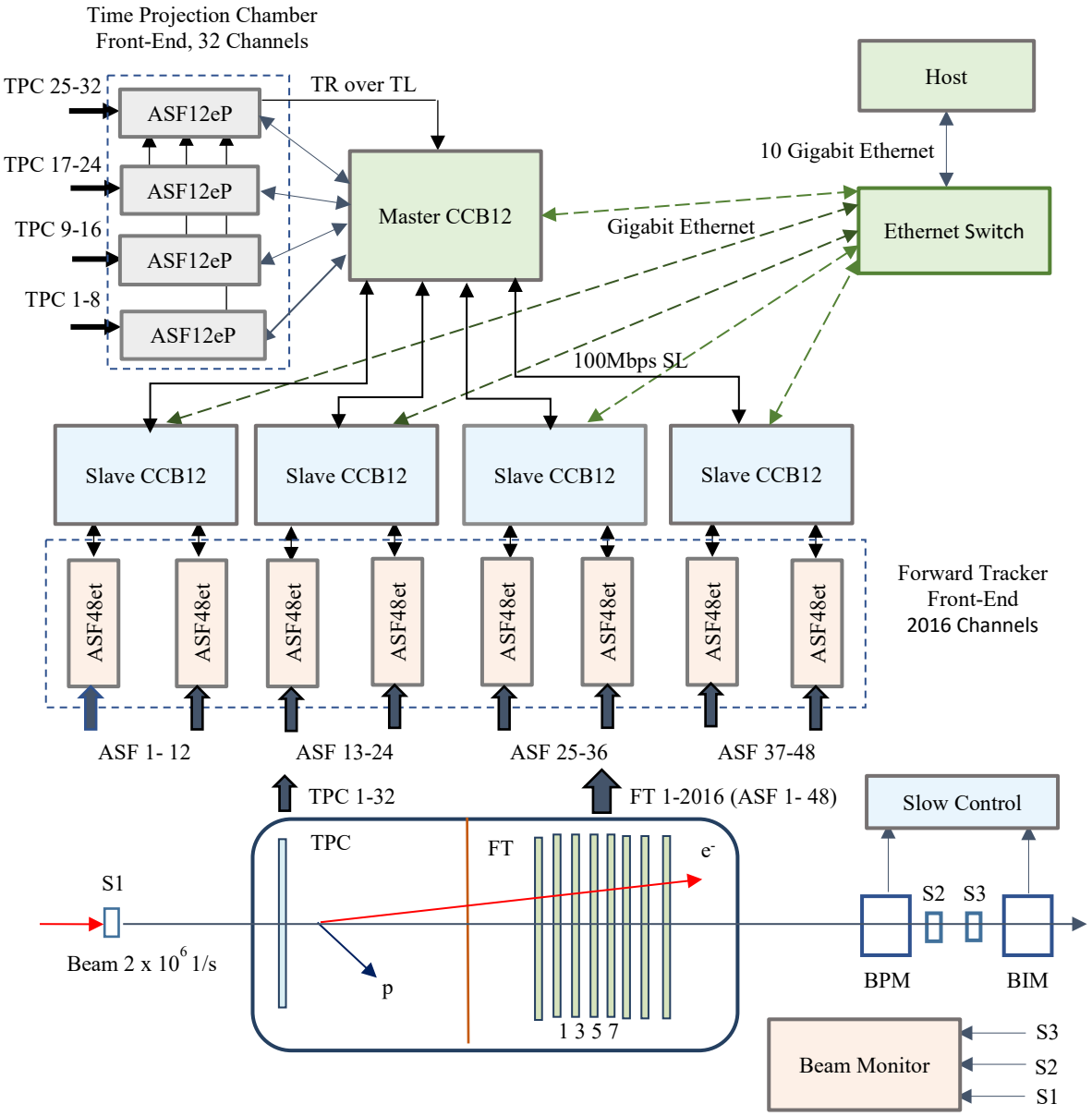

Fig. 1. Schematic view of the experimental set-up and the data acquisition system

The TPC anode is segmented into the central pad and eight concentric rings along the radius, some rings are subdivided into sectors. The total number of channels for the TPC anode readout reaches 32. The target parameters for the measurement are the energy of the recoil proton and the signal arrival time.

The FT consists of four pairs of chambers that measure the X and Y coordinates of the scattered electron track relative to the beam line. Each chamber is a symmetrical multiwire proportional chamber 600×600 mm^2 in size with an anode plane (wires with a pitch of 3 mm) between two cathode planes (wires with a pitch of 0.5 mm). The cathode wires are orthogonal to the anode wires in one cathode plane (X or Y) and are inclined at an angle of 45° in the other cathode plane (U). Every five wires in the orthogonal cathode plane are grouped into strips. The strip in an inclined cathode plane consists of 100 wires. The number of signal channels in each chamber is 240 + 12 = 254, which gives a total of 2016 channels for eight chambers. The target parameters for the measurement are the centre of gravity and the time of arrival of the cathode signal(s).

Beam monitoring is based on S1... S3 scintillation counters, a high-pressure ionization chamber as a beam intensity monitor (BIM) and a small proportional chamber as a beam position monitor (BPM). Knowing the number of beam electrons is necessary to determine the absolute cross section. The beam intensity is expected to be $2 \cdot 10^6$ electrons per second.

This article only deals with receiving events from the TPC and FT detectors and does not cover the electronics of the beam monitoring detectors. The detection of both the recoil proton and the scattered electron makes it possible to reconstruct the *ep* scattering event.

Using a flash analog-to-digital converter (flash ADC) is best suited to measure the target parameters of both detectors. The data acquisition system for the above two detectors has a tree-like architecture and is based on a configurable amplifier–shaper–flash (ASF) ADC, multichannel digitizer and a 12-port concentrator–control–board (CCB12). The CCB12 distributes the system clock and commands from the host computer to downstream devices over serial links (SL). The SL connects serial ports (SP) of the upstream and downstream devices and operates at 100 Mbps in both directions. A special class of broadcast commands addressed to the Master CCB12, such as “start operation”, “stop operation”, or generated by the Master CCB12, such as “trigger”, eventually reaches each device in the acquisition tree, causing them to work synchronously.

Registration of a recoil proton in any of the TPC channels causes a trigger request (TR) signal to be sent over the trigger link (TL) to the Master CCB12, the latter may distribute it as a “trigger” command.

Upon receiving a “trigger”, each channel of the TPC and FT digitizers generates a data block, containing event(s). An event is an array of flash ADC readings obtained as a result of digitizing the detector signal.

For offline event synchronization, each event in the data block is timestamped. The timestamp is a 44-bit binary counter that starts running in each device on the “start run” command. The counter overflow occurs after approximately 48 h. This makes the timestamp the unique identifier for the event. The CCB12 multiplexes twelve input 100 Mbps data streams into one and sends it to an Ethernet switch over Gigabit Ethernet. The switch communicates with the host *via* the 10 Gigabit Ethernet.

Digitizer. Two versions of the digitizer, called ASF12eP and ASF48et, serve the TPC and FT detectors, respectively. Both versions use the same ASF_48et main board design. It contains six flash ADC chips and programmable logic in the Spartan-6 LX field-programmable gate array (FPGA), see Fig. 2. For greater flexibility, the amplifiers and shapers are placed on a separate daughter board, which is connected to the input sockets on the main board.

The flash ADC chip is a 12-bit high-performance, low-power, octal channel analog devices ADS5282 ADC with a differential input voltage in the 2 V range and low-voltage differential signaling (LVDS) output. The input sampling rate can vary from 10 to 65 megasamples per second (MSPS). The output data latency is 12 sampling clock cycles. The serialized double data rate (DDR) outputs run at 6 times the input clock.

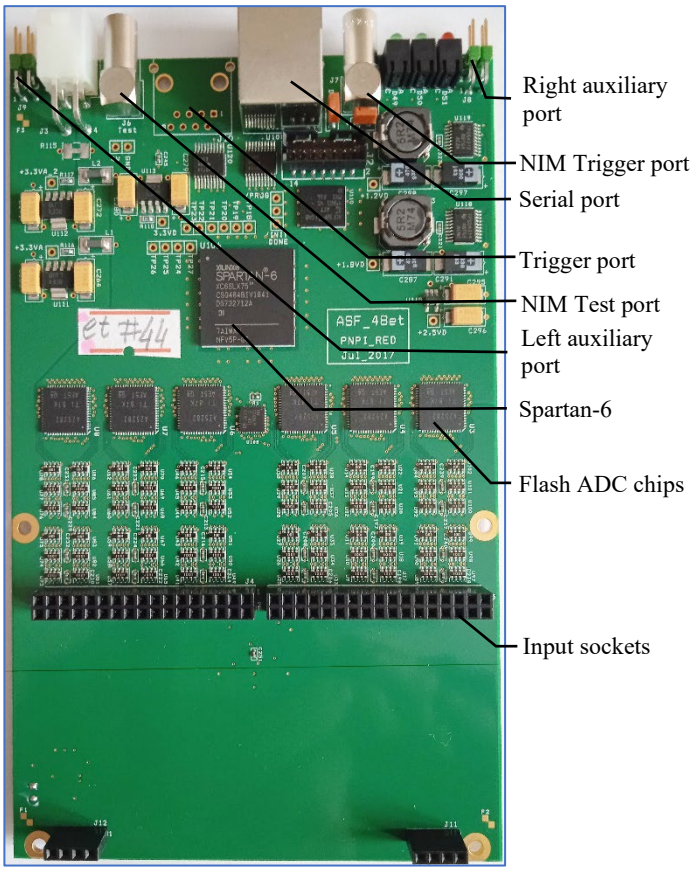

Fig. 2. ASF_48et close up

The Spartan-6 LX FPGA pinouts are 100% compatible across density in the same package. Thus, depending on the requirements, the ASF_48et board can be equipped with either the cheapest LX45 FPGA, or the more expensive LX75 and LX100 FPGAs, or the most expensive LX150 FPGA. All ports: SP for receiving commands and uploading data blocks, trigger port (TP) for sending TR to Master CCB12, NIM (NIM – current-based logic defined in nuclear instrumentation module standard) test port for receiving test signals, left and right auxiliary ports (LAP, RAP) for signal exchange between digitizers – are controlled *via* the FPGA. This data acquisition system does not use the NIM TP to receive external "trigger" signals. The signal standard for all ports except NIM is differential LVDS.

Concentrator. The CCB12 design is made as a main and daughter board, see Fig. 3. The main board has 12 SPs one upstream SP (USP) and TP. All ports use RJ45 connectors. The SLs connecting SPs or TPs of upstream and downstream devices are category 5e shielded patch cords. An inexpensive Spartan-3 FPGA on the main board controls all ports. The daughter board connects to the main board *via* a 96-pin connector. The daughter board is an off-shelf product TE0720-03-1CFA from Trenz Electronic GmbH. It integrates a Xilinx Zynq XC7Z020 system-on-chip (SoC), a Gigabit Ethernet transceiver, 1 GB DDR3 synchronous dynamic random access memory (DDR3 SDRAM), and 32 MB flash memory for configuration and operation. The SoC includes user-programmable resources: an Artix-7 FPGA and a dual-core ARM Cortex-A9 processor, on which all concentrator operation algorithms are built. The two versions of the concentrator, called Master CCB12 and Slave CCB12, use the same hardware but differ in firmware and processor codes.

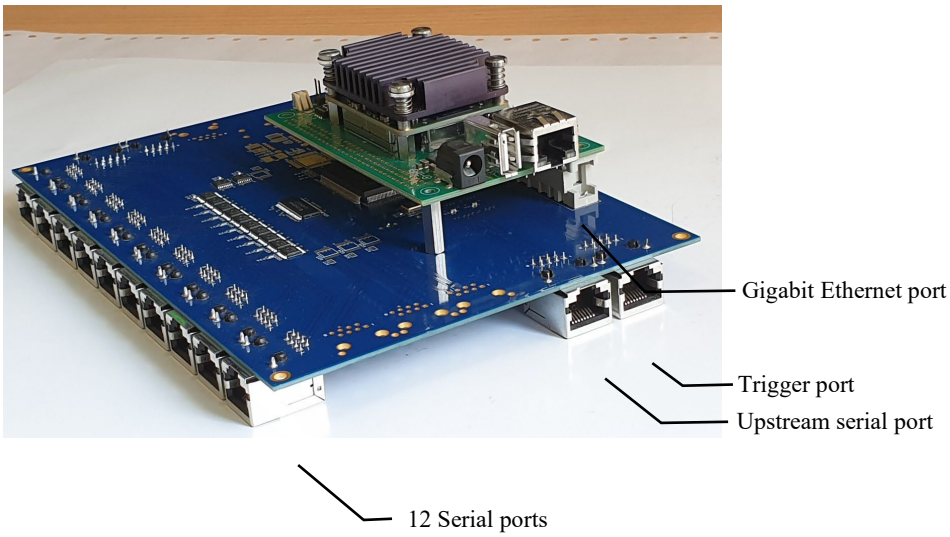

Fig. 3. Concentrator CCB12

ASF12eP digitizer. The ASF12eP digitizer collects data from the TPC. The TPC maximum drift time is 100 μs, but the spread of the signal arrival time from anode segments does not exceed 25 μs. To get a complete picture of the recoil proton track, the digitizers collect data from all segments of the anode in a 40 μs window. The chosen 25 MHz sampling rate is a compromise between obtaining optimal time resolution (40 ns), the number of readings per "trigger" (typically 1 000 readings, but can be increased to 4 000 readings) and the expected "trigger" rate of 50 Hz. To further minimize the SL load and dead time, the number of channels has been reduced from a potentially available 48 to 12. Low-noise, charge-sensitive preamplifiers with a peaking time of 1 μs have a noise level of 13 keV + 0.5 keV/pF and can measure TPC signals from 250 keV up to 5 MeV.

The main board has a Spartan-6 LX100 FPGA. The logic for each digitizer channel includes:

- Deserializer of flash ADC serial output into a parallel word;
- 12-bit signal amplitude discriminator;
- 18-bit moving integrating window (MIW);
- 15-bit MIW discriminator;
- Oipeline delay to compensate for "trigger" latency;
- 8K word first-in-first-out (FIFO) memory that serves as the channel's derandomizing buffer.

The MIW width can be up to 127 readings. The integrator works with the 11 most significant bits (MSB) of the flash ADC reading. On each sampling clock cycle, it adds a new reading and subtracts the earliest in time. The MIW discriminator compares the 15 MSB of the integrator with a threshold.

The outputs of the amplitude discriminator or MIW discriminator in any channel, or their coincidence, can be the source of the TR signal. TR is available at LAP or RAP. One of the four ASF12ep digitizers collects all TR *via* logical OR and sends them *via* TL to the TP of the Master CCB12, and the Master CCB12 broadcasts it as a "trigger" to all devices. Upon receiving a "trigger", each channel of the digitizer generates an event with a timestamp corresponding to the time the "trigger" arrived. Events from all channels are combined into a common 32K word FIFO, which serves as a device derandomizing buffer and forms a single output data stream. Typically, TR generation is enabled for the second or third ring segments of the anode, *i. e.* delayed relative to the beginning of the track. To compensate for the delay, the event window typically begins 15 μs before the "trigger" and ends 25 μs after it, but can be adjusted over a wide range.

ASF48et digitizer. The ASF48et digitizer collects data from the FT. Any electron track found in the FT (outside the central dead zone of 2 cm) in the time window 100 μs before the "trigger" signal could be the parent particle of the recoil proton. The digitizer is equipped with low-noise, charge-sensitive preamplifiers with a peaking time of 1 μs and a noise level of 0.072 fC + 0.0015 fC/pF.

The main board has a Spartan-6 LX75 FPGA. The logic for each digitizer channel includes:

- Deserializer of flash ADC serial output into a parallel word;
- Signal amplitude discriminator;

- Pipeline delay to compensate for “self-trigger” latency;
- 1K word memory as a ring buffer.

Each channel operates in self-triggered mode. Self-triggering causes the event to be stored in the ring buffer. Each event contains a timestamp corresponding to the time the “self-trigger” arrived and an array of flash ADC readings (typically 80 readings, but can be increased to 960 readings). The time position of the event is chosen to include both baseline and maximum amplitude readings. Both are used to find the centre of gravity (coordinate) of the scattered electron. Upon receiving a “trigger”, self-triggered events from all channels that occurred in the 100 μs time window preceding the “trigger” are reloaded into a 16K word output FIFO to eventually form a single output data stream.

Master CCB12 and Slave CCB12 concentrator. The Master has a built-in trigger logic that receives TR signals from the ASF12eP digitizer and sends “triggers” to other devices in the acquisition tree. It assigns a timestamp to each received TR and marks it if it is used to generate a “trigger”. The “trigger” information constitutes the 13th data stream in addition to the 12 data streams coming from the SPs. The Master also distributes broadcast commands from the host to all downstream devices. It has different logic for the SP connected to the digitizer and the SP connected to the Slave, because it does not receive any data from the Slave, only its busy status, which is used in the trigger logic.

Both types of concentrators have the same logic for the SP connected to the digitizer. Two special commands “hold” and “resume” control the flow of data between digitizers and concentrators: “hold” causes the digitizer to stop sending data, and “resume” resumes normal data flow. The 16K word FIFO at the input of each SP serves as the channel’s derandomizing buffer. The FPGA logic reloads the data from the input FIFO to the 32K word output FIFO, splitting it into packets with headers and trailers. The header and trailer added to the packet contain overhead information such as header timestamp, packet number, SP number, number of kilo-words loaded into input and output FIFOs, trailer timestamp, and checksum. The processor forwards packets from the output FIFO to the host *via* Gigabit Ethernet.

The data acquisition system for the “Proton” experiment has been tested on cosmic rays.

References

1. A.A. Vorobyev *et al*. PNPI. High Energy Physics Division. Main Scientific Activities 2013–2018, 316–325 (2019).