UNIVERSITY OF FLORIDA–PNPI HIGH VOLTAGE SYSTEM IN THE CMS ENDCAP MUON DETECTOR

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The design and construction of the University of Florida (UF) – PNPI high voltage system (HVS) was performed in collaboration with specialists of the UF [1] for three detecting stations ME1/2, ME1/3, ME2, ME3, and ME4 of each of the two endcaps in the CMS endcap muon system (EMU) [2]. In total, there are 234 cathode strip chambers (CSC) per each endcap as it is shown in Fig. 1. The detecting stations are divided into two regions each: ME1/2 and ME1/3, ME2, 3, 4/1 and ME2, 3, 4/2. At present, there are 468 six-plane CSC. Each plane should be provided with a high voltage (HV) line. Moreover, the HV line in each layer is subdivided into several segments (Fig. 2). Five segments are in the chambers ME2/2, ME3/2, ME4/2, and 3 segments are in all other chambers.

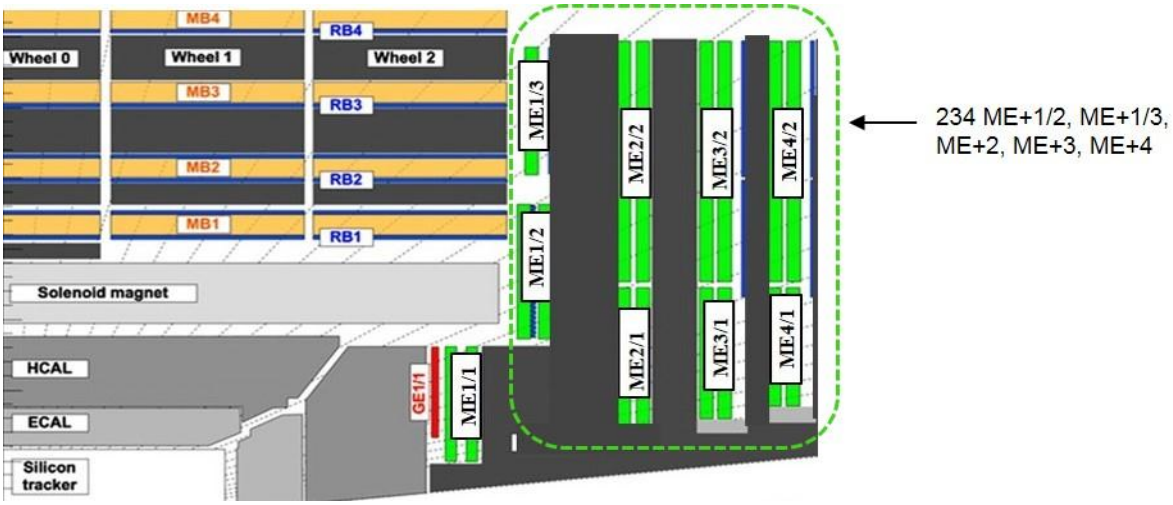

Fig. 1. Structure of the CMS endcap muon system

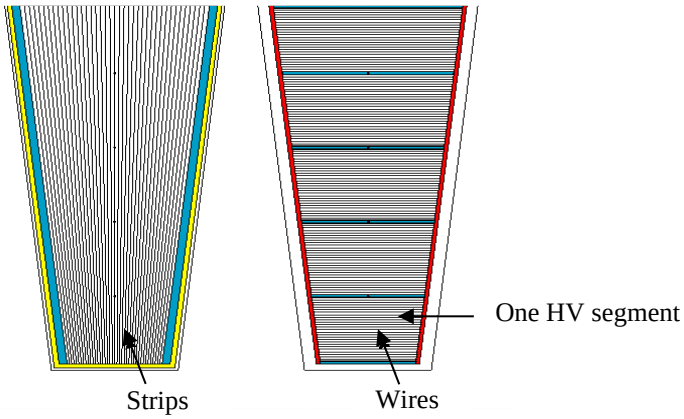

Fig. 2. Structure of the CSC with five HV segments

The main purpose of the HVS is to provide high voltage for the CMS endcap CSCs. CSC features that affect the HVS design are the following:

- small HV segments and high tolerance to HV failures,
- the same working voltage with small variation from segment to segment,
- a problematic segment can be fixed by reducing voltage or disconnecting from HV,

- precise consumption current for each segment,
- detects discharges and leaks.

Figure 3 shows the overall hierarchical structure of the HV distribution in the HVS.

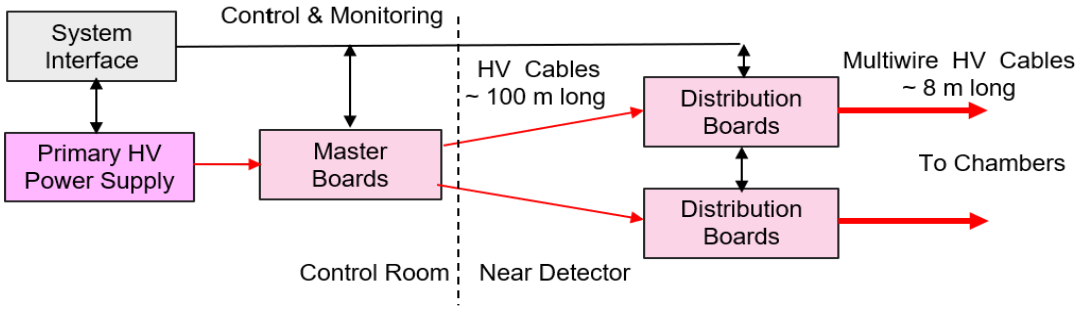

Fig. 3. HVS distribution structure

The custom-made HVS has a three-tier structure. There are eight commercial Matsusada primary HV power supplies (PHVPS). They provide the HV power to 50 master boards, each of which has eight regulated outputs. Both the PHVPS and the crates with the master boards are located in underground service cavern (USC). The master board outputs are routed to the distribution boards located near CSCs (on the periphery of the endcap discs). There are two types of distribution boards: 216 30-channel boards serve ME2/2, ME3/2, ME4/2 chambers (one chamber per board); 126 36-channel boards serve ME2/1, ME3/1, ME4/1, ME1/2, ME1/3 chambers (two chambers per board). The system interface consists of a control computer and control boards, which provide control and monitoring operation for each channel of the HVS. Table 1 summarizes the quantities of different hardware components in the HVS.

Table 1

Summary of hardware components in the HVS

Component	Quantity
Primary high voltage power supply	8
Control computers	2
Low voltage power supplies	2
Control boards	4
Master boards	50
Distribution boards, 30 channels	216
Distribution boards, 36 channels	126
Independently regulated and monitored distribution channels	11 016

There are eight PHVPSs in the system. All of them are located in the control room. Each of these modules supplies high voltage to one of eight partitions of the HVS. PHVPS is a commercially available module, manufactured by Matsusada Precision with the following parameters:

- AU-5P60-LF(U) HV power supply, 5 000 V / 60 mA;
- GP-HV-L(U) control interface;
- RS-232C module for control interface.

The master boards are located in the control room, and they receive HV generated by PHVPS and distribute it to its eight outputs. Each output is independent and capable of

- regulate voltage from 0 to 4 000 V,
- deliver up to 1.5 mA of current into the load,
- voltage measurement from 0 to 4 000 V,
- current measurement from 0 to 1.5 mA,
- over-voltage and over-current protection with programmable threshold.

The distribution boards are located in underground experimental cavern (UXC), in racks near the discs, to minimize the length of the cables that deliver voltage from them to all chambers. Each distributor board receives high voltage from the master board *via* very long cable and distributes it to its 30 or 36 outputs. Each output of a distribution board is independent and capable of

- regulate voltage up to 1 000 V down from maximum voltage supplied from the master board output,
- deliver up to 100 mkA of current into the load,
- voltage measurement from 0 to 4 000 V,
- current measurement from 0 to 100 mkA,
- over-voltage and over-current protection with programmable thresholds and timeouts.

Each distribution board output provides power for one HV segment of a CSC.

Two computers control the entire HVS. Both computers are located in USC. Figure 4 shows the software structure and control interfaces of the HVS. The software was designed and maintained by specialists of the UF.

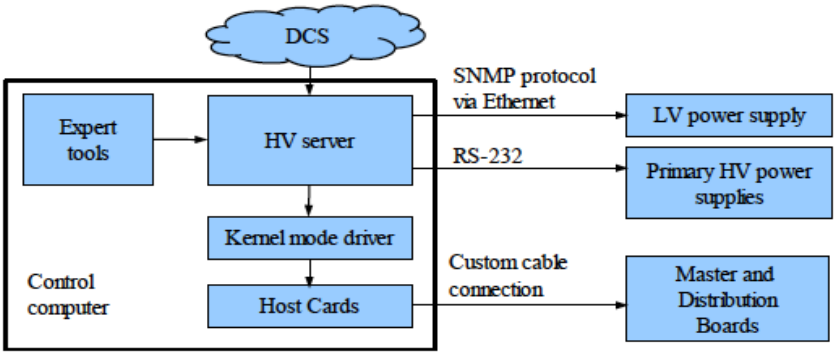

Fig. 4. Software structure and control interfaces of the HVS

The HV server is based on the distributed information management (DIM) system [3] and performs the following tasks:

- receives high-level commands from detector control system graphical user interface or from expert tools;
- decodes these commands; passes the corresponding parameters to the kernel mode driver, the PHVPS and the low voltage power supply (LVPS);
- reads out and publishes the monitoring information from all master and distribution boards, the PHVPS and the LVPS.

The main purpose of the kernel mode driver is to provide control and monitoring of the master and distribution boards in real time:

- over-current and over-voltage trips,
- voltage ramp-up and ramp-down,
- pre- and post-trip data logging for future analysis.

There are several standalone expert tools that can be run on the HVS control computer. They provide control of one or multiple components of the system including:

- displaying voltages, currents, voltage and current trip levels and timeouts, states of all channels of the selected component;
- setting any of the above parameters using simple command-line interface;
- each channel calibration for voltage setting, voltage, and current sensors;
- trip profile analysing in case of overcurrent or overvoltage.

As a result, the HVS has a developed hardware and software basis to provide stable operation for a number of years. Table 2 shows the number of channel and board failures by years. Elevated failures in 2009 are due to the replacement operation of the batch of resistors with unstable parameters. Elevated failures in 2014 are due to the system upgrade with new boards installation for ME4/2.

Table 2

HVS channel and board failures

Year	Distribution board – 36		Distribution board – 30		Master board	
	Single channel	Board	Single channel	Board	Single channel	Board
2009	23	1	30	2	3	1
2010	11	1	4	0	0	0
2011	4	16	6	1	1	1
2012	4	1	2	1	0	0
2013	0	0	0	0	0	0
2014	0	1	6	6	2	1
2015	2	0	0	0	2	1

Figure 5 shows the voltage calibration stability in time during one year. The drift is negligible. The voltage calibrations are now tested periodically for all channels.

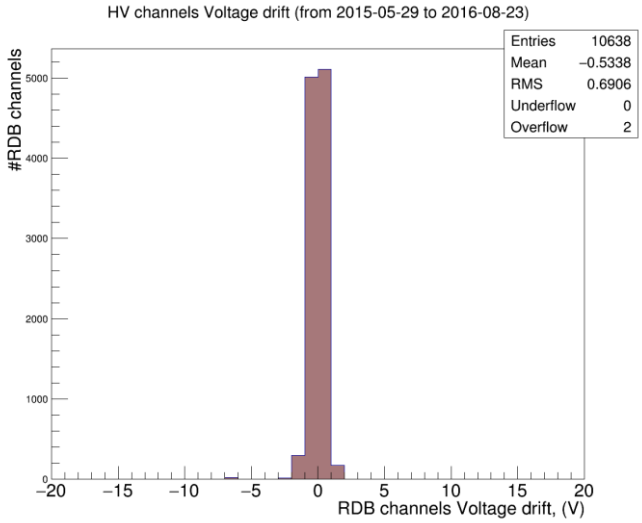

Fig. 5. HVS high voltage channels drift in time

References

1. A.A. Vorobyov *et al.*, *PNPI. High Energy Physics Division. Main Scientific Activities 2002–2006*, Gatchina, 2007, pp. 26–34.
2. A.A. Vorobyov *et al.*, *PNPI. High Energy Physics Division. Main Scientific Activities 2007–2012*, Gatchina, 2013, p. 27.
3. DCS Users Manual, https://twiki.cern.ch/twiki/bin/view/CMS/CSCOperationsDCS