THIRD GENERATION COORDINATE READOUT SYSTEM – CROS-3

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The design and development of the fast and cost effective readout electronics for the tracking detectors is the scope of interest of the modern experiments such as LAND (performed at GSI, Darmstadt), FAMILON, *etc*. The setup of the experiments includes fine pitch MultiWire Proportional Chambers (MWPC) and wire Drift Chambers (DC) with hexagonal cell structure. Variety of modern integrated circuits together with advanced PCB technology allowed to develop the best quality CROS-3 devices and meet the requirements of the experiments.

Block diagram of the CROS-3 system in Fig. 1 includes:

- 96-channel MWPC Digitizers (CDR96);
- 16-channel DC Digitizers (AD16);
- 16-channel Concentrators (CCB16);
- System Buffer (CSB).

Analog part of the CDR96 is based on a CMP_G ASIC performing wire signal amplification and shaping as well as pulse discrimination with peaking time of 30 ns, minimum threshold of 7 fC, double pulse resolution of 80 ns, and power dissipation about 35 mW/channel.

Analog part of the 16-channel DC Digitizer is based on a ASD-Q ASIC [1] with similar functionality and the following characteristics: peaking time of 7 ns, operational threshold at 2–3 fC, double pulse resolution of 20 ns, and power dissipation about 35 mW/channel.

Digital part of either Digitizer is implemented in a Xilinx Spartan-3 FPGA that performs both digitization and readout tasks. Input signals are digitized and delayed to compensate for the trigger latency. Upon receiving a trigger signal, a temporary buffer stores programmable number of time bins. Then the encoder looks for the signal leading edge and encodes both its wire number and its relative time slice number. The delay range compensates trigger latency of up to 2.5 μs in 10 ns steps. The finest time bin resolution is 2.5 ns for the AD16 and 10 ns for the CDR96 cards. Maximim number of time slices is 255 for AD16 and 64 for CDR96. Readout is performed over a STP CAT5 cable at a 100 Mb/sec bit rate.

The CCB16 collects data from up to 16 Digitizers into temporary buffers, which are read out to the CSB via an optical fibre at a 2.0 Gb/sec bit rate.

The CSB is implemented as a universal PCI card.

Figure 2 shows system components mounted directly on the chamber.

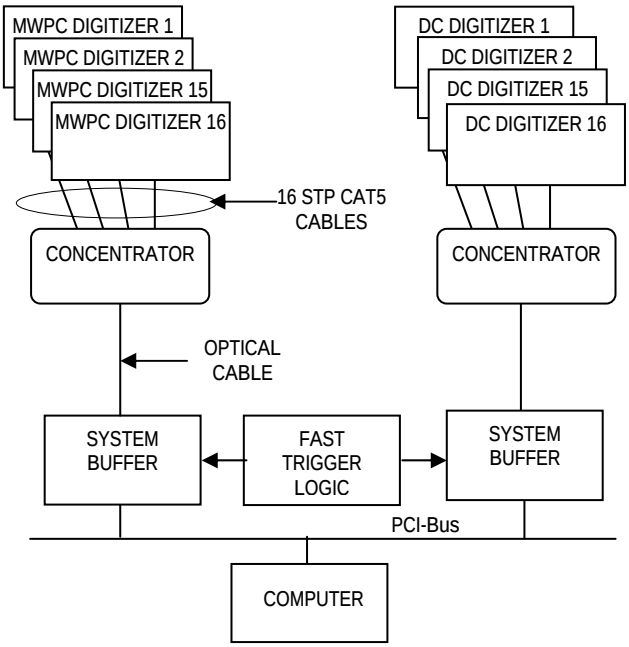

Fig. 1. CROS-3 block diagram

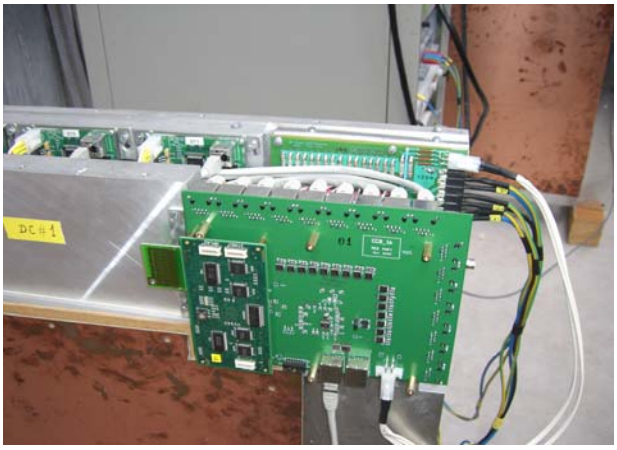

Fig. 2. CROS-3 Digitizers and Concentrator are on-chamber mounted system components

References

1. W. Bokhari *et al.*, CDF/DOC/TRACKING/CDFR/4515 December 1999.